CLAIMS

1. A device having a clock generation circuit which produces a first clock signal for use in timing internal circuitry and a second clock timing circuitry that interfaces to external circuitry, the clock generation circuit comprising:

a) a phase locked loop having an output,

b) a first programmable frequency scaling circuit having an input coupled to the output of the phase locked loop, an output of the first programmable frequency scaling circuit providing the first clock signal; and

c) a second programmable frequency scaling circuit having an input coupled to the output of the phase locked loop, an output of the second programmable frequency scaling circuit supplying the second clock signal.

2. The device of claim 1 additionally comprising:

a) digital logic receiving as a clock input the first clock; and

b) interface logic, interfacing to the digital logic components external to the device and receiving as a clock input the second clock signal.

3. The device of claim 1 wherein the first programmable frequency scaling circuit is a first programmable divider and the second programmable frequency scaling circuit is a second programmable divider.

4. The device of claim 3 wherein the first programmable divider is a first programmable counter and the second programmable divider is a second programmable counter.

5. The device of claim 3 additionally comprising control logic providing control signals to the first programmable divider and the second programmable divider.

6. The of claim 5 wherein the control logic provides to the first programmable divider, control signal controlling the loading of a programmed divider value, when the control logic detects an end of a period of the first clock.

7. The device of claim 6 wherein the first programmable divider stores a programmable divider value and upon loading a new programmed divider value in the first programmable divider, the control logic generates an enable control signal to the first programmable divider causing the first programmable divider to hold its output until the second clock reaches a transition.

8. The device of claim 3 wherein the phase locked loop additionally comprises a third programmable divider.

9. The device of claim 1 wherein the device comprises a semiconductor chip and the semiconductor chip additionally comprises at least one control register with fields specifying the scale factor of the first frequency scaling circuit and the second frequency scaling circuit.

10. A method of operating a data processing chip having first circuitry and circuitry that interfaces to devices external to the data processing chip, comprising:

a) providing a reference clock;

b) specifying a first frequency ratio between the first clock and the reference clock;

c) deriving a first clock from the reference clock with the first frequency ratio;

d) specifying a second frequency ratio between the second clock and the reference clock, the second frequency ratio specified independent of the first frequency ratio;

e) deriving a second clock from the reference clock with the second frequency ratio;

f) clocking circuitry within the first circuitry using the first clock and clocking circuitry that interfaces to devices external to the core circuitry with the second clock.

11. The method of operating a data processing chip of claim 10 additionally comprising changing the frequency of the first clock on the fly.

12. The method of operating a data processing chip of claim 10 additionally comprising placing the chip in a first power saving mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate.

13. The method of operating a data processing chip of claim 12 additionally comprising placing the chip in a second power saving mode by reducing the frequency of the reference clock.

14. The method of operating a data processing chip of claim 12 wherein the data processing chip processes data in a mobile telephone and placing the chip in a first power saving mode occurs while a call is in process on the mobile telephone.

15. The method of operating a data processing chip of claim 13 wherein the data processing chip is inside a mobile telephone and placing the chip in a second power saving mode occurs while the mobile telephone is not in use to make a call.

16. The method of operating a data processing chip of claim 10 additionally comprising placing a chip in a first power savings mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate without changing the frequency of the reference clock or the second clock.

17. The method of operating a data processing chip of claim 10 wherein the frequency of the first clock and the frequency of the second clock are not integer multiples of each other.

18. The method of operating a data processing chip of claim 10 wherein the data processing chip comprises at least one control register with fields specifying the frequency ratio between the reference clock and the first clock and between the reference clock and the second clock.

19. A method of operating a data processing chip having first circuitry and circuitry that interfaces to devices external to the first circuitry wherein the first circuitry is clocked with a first clock and the circuitry that interfaces to devices external to the core is clocked with a second clock, the frequency of the first clock and the second clock being controllable, the method comprising:

a) loading a control location with a first value that controls the frequency of the first clock;

b) loading a control location with a second control value that controls the frequency of the second clock;

c) providing a new value for at least one of the first clock and the second clock;

d) waiting until a defined time relative to the period of the second clock while holding the state of the first clock; and

e) loading the new value in a control location at the defined time.

20. The method of claim 19 wherein the second clock operates at a slower frequency than the first clock.

21. The method of claim 20 wherein the data processing chip processes data in a mobile telephone and providing a new value for one of the first clock and the second clock comprises providing a new value for the first clock while a call is in process on the mobile telephone.

22. The method of claim 19 wherein providing the new value for one of the first clock and the second clock comprises setting a value in a control register.

23. The method of claim 22 wherein loading a control location comprises loading a location in a programmable counter.

24. The method of claim 19 wherein the data processing chip is used in a battery operated electronic device and the new value is provided for the first clock to place the electronic device in a power saving mode.

25. The method of claim 24 additionally comprising, replacing the new value stored in the control location with the first value to take the electronic device out of power saving mode.